AMENDMENTS TO THE CLAIMS

This listing of claims will replace all prior versions and listings of claims in the application:

Claim 1 (Currently Amended):

An electronic circuit for self-test of a random access memory array having a plurality of memory storage cells in a RAM circuit, wherein the storage cells are organized into a plurality of slice arrays, comprising:

a control circuit, wherein the control circuit is embedded in a control and address block of the RAM circuit;

an address selection circuit, wherein the control circuit directs the address selection circuit to index through memory addresses;

one input/output circuit each associated with each slice array, wherein the control circuit directs each input/output circuit to write data into its associated slice array at an indexed memory address, to read data from the associated slice array at the indexed memory address, and to compare the data read from the associated slice array with that written into the associated slice array at the indexed memory address; and

an error detection circuit, wherein the error detection circuit collects results of self-test data comparisons from each input/output circuit and notifies the control circuit of the results of the self-test data comparisons, wherein:

when a defect is present in one of the slice arrays, the input/output circuit associated with the defective slice array redirects data intended for storage in the defective slice array to an adjacent slice array of the defective slice array,

otherwise, the input/output circuit associated with the slice array directs data intended for storage in the slice array to the slice array,

and wherein:

when a defect is present in one of the slice arrays, the input/output circuit associated with the defective slice array redirects data read from the adjacent slice array of the defective slice array to the output of the defective slice array,

otherwise, the input/output circuit associated with the slice array directs data read from the slice array to the output of the slice array.

Claim 2 (Original):

The electronic circuit as recited in claim 1, wherein the electronic circuit is embedded within the RAM circuit in an integrated circuit.

Claim 3 (Previously Presented):

The electronic circuit as recited in claim 1, wherein the address selection circuit is embedded in the control and address block of the RAM circuit.

Claim 4 (Original):

The electronic circuit as recited in claim 1, wherein the control circuit initiates and terminates the self-test at preselected conditions, wherein the address selection circuit, informs the control circuit when the indexed memory address equals an initial self-test memory address, and wherein the address selection circuit, informs the control circuit when the indexed memory address equals a final self-test memory address.

Claim 5 (Currently Amended):

~~The electronic circuit as recited in claim 1,~~ An electronic circuit for self-test of a random access memory array having a plurality of memory storage cells in a

RAM circuit, wherein the storage cells are organized into a plurality of slice arrays, comprising:

a control circuit, wherein the control circuit is embedded in a control and address block of the RAM circuit;

an address selection circuit, wherein the control circuit directs the address selection circuit to index through memory addresses;

one input/output circuit each associated with each slice array, wherein the control circuit directs each input/output circuit to write data into its associated slice array at an indexed memory address, to read data from the associated slice array at the indexed memory address, and to compare the data read from the associated slice array with that written into the associated slice array at the indexed memory address; and

an error detection circuit, wherein the error detection circuit collects results of self-test data comparisons from each input/output circuit and notifies the control circuit of the results of the self-test data comparisons and wherein the address selection circuit comprises:

an address multiplexer, wherein the address multiplexer has first, second, and third address-multiplexer inputs and an address-multiplexer output, wherein the second address-multiplexer input receives the memory address at which the self-test is initiated, wherein the third address-multiplexer input is configured to receive normal operational data addresses, and wherein when the address multiplexer receives command from the control circuit to initiate the self-test, the value of the second address-multiplexer input is transferred to the address-multiplexer output;

a register, wherein the address-multiplexer output is connected to the input of the register and wherein the content of the

register is used to address the RAM memory in writing and reading self-test data;

a sequencer, wherein the output of the register is connected to the input of the sequencer, wherein the sequencer outputs an indexed version of the address received at the input of the sequencer, and wherein the output of the sequencer is connected to the first address-multiplexer input; and

a comparator, wherein the output of the register is connected to the input of the comparator, wherein the comparator has first and second comparator outputs, wherein comparator first and second outputs are connected to the control circuit, wherein the first comparator output indicates when the register contains an initial self-test memory address, and wherein the second comparator output indicates when the register contains a final self-test memory address.

Claim 6 (Original):

The electronic circuit as recited in claim 5, wherein the address multiplexer, the register, the sequencer, and the comparator are embedded in a control and address block of the RAM circuit.

Claim 7 (Currently Amended):

~~The electronic circuit as recited in claim 1,~~ An electronic circuit for self-test of a random access memory array having a plurality of memory storage cells in a RAM circuit, wherein the storage cells are organized into a plurality of slice arrays, comprising:

a control circuit, wherein the control circuit is embedded in a control and address block of the RAM circuit;

an address selection circuit, wherein the control circuit directs the address selection circuit to index through memory addresses;

one input/output circuit each associated with each slice array, wherein the control circuit directs each input/output circuit to write data into its associated slice array at an indexed memory address, to read data from the associated slice array at the indexed memory address, and to compare the data read from the associated slice array with that written into the associated slice array at the indexed memory address; and

an error detection circuit, wherein the error detection circuit collects results of self-test data comparisons from each input/output circuit and notifies the control circuit of the results of the self-test data comparisons and wherein the input/output circuit comprises:

a data-in multiplexer, wherein the data-in multiplexer has first and second data-in-multiplexer inputs and a data-in-multiplexer output, wherein the first data-in-multiplexer input is configured to receive the self-test data, wherein the second data-in-multiplexer input is configured to receive normal operational data, and wherein:

when the data-in multiplexer receives command from the control circuit to perform the self-test, the value of the first data-in-multiplexer input is transferred to the data-in-multiplexer output,

otherwise, the second data-in-multiplexer input is configured to transfer its value to the data-in-multiplexer output;

an input register, wherein the output of the data-in-multiplexer output is connected to the input of the input register;

an inverter, wherein the output of the input register is connected to the input of the inverter;

an input-complement multiplexer, wherein the input-complement multiplexer has first and second input-complement-multiplexer inputs and an input-complement-multiplexer output, wherein the output of the input register is connected to the first input-complement-multiplexer input, wherein the output of the inverter is connected to the second input-complement-multiplexer input, and wherein:

when, the control circuit instructs the input-complement multiplexer to write test data into the slice array, the value of the first input-complement-multiplexer input is transferred to the input-complement-multiplexer output,

otherwise, the value of the second input-complement-multiplexer input is transferred to the input-complement-multiplexer output;

an 'output-complement multiplexer, wherein the output-complement multiplexer has first and second output-complement-multiplexer inputs and an output-complement-multiplexer output, wherein the output of the input register is connected to the first output-complement-multiplexer input, wherein the output of the inverter is connected to the second output-complement-multiplexer input, and wherein:

when the control circuit instructs the output-complement multiplexer to compare test data to data in the slice array, the value of the first output-complement-multiplexer input is transferred to the output-complement-multiplexer output,

otherwise, the value of the second output-complement-multiplexer input is transferred to the output-complement-multiplexer output;

an output register, wherein the output register receives the contents of the slice array; and

an exclusive-OR gate, wherein the exclusive-OR gate has first and second exclusive-OR-gate inputs and an exclusive-OR-gate output, wherein the output of the output register is connected to the first exclusive-OR-gate input, and wherein the output-complement-multiplexer output is connected to the second exclusive-OR-gate input.

Claim 8 (Original):

The electronic circuit as recited in claim 7, wherein the input to the error detection circuit is connected to the exclusive-OR-gate output.

Claim 9 (Canceled):

Claim 10 (New):

The electronic circuit as recited in claim 1, wherein when a defect is present in one of the slice arrays, the input/output circuit associated with each subsequent slice array of the defective slice array redirects data intended for storage in that subsequent slice array to the adjacent slice array of that subsequent slice array and the input/output circuit associated with each previous slice array of the defective slice array directs data intended for storage in that previous slice array to that previous slice array and wherein when a defect is present in one of the slice arrays, the input/output circuit associated with each subsequent slice array of the defective slice array redirects data read from the adjacent slice array of that subsequent slice array to the output of that subsequent slice array and the input/output circuit associated with each previous slice array of the defective slice array directs data read from that previous slice array to the output of that previous slice array.

Claim 11 (New):

The electronic circuit as recited in claim 5, wherein the electronic circuit is embedded within the RAM circuit in an integrated circuit.

Claim 12 (New):

The electronic circuit as recited in claim 5, wherein the address selection circuit is embedded in the control and address block of the RAM circuit.

Claim 13 (New):

The electronic circuit as recited in claim 5, wherein the control circuit initiates and terminates the self-test at preselected conditions, wherein the address selection circuit, informs the control circuit when the indexed memory address equals an initial self-test memory address, and wherein the address selection circuit, informs the control circuit when the indexed memory address equals a final self-test memory address.

Claim 14 (New):

The electronic circuit as recited in claim 7, wherein the electronic circuit is embedded within the RAM circuit in an integrated circuit.

Claim 15 (New):

The electronic circuit as recited in claim 7, wherein the address selection circuit is embedded in the control and address block of the RAM circuit.

Claim 16 (New):

The electronic circuit as recited in claim 7, wherein the control circuit initiates and terminates the self-test at preselected conditions, wherein the address selection circuit, informs the control circuit when the indexed memory address equals an initial self-test memory address, and wherein the address selection circuit, informs the control circuit when the indexed memory address equals a final self-test memory address.